REMARKS

Claims 1 through 39 are currently pending in the application. Claims 1, 14, and 27 have been amended.

Claims 7 through 11, 20 through 24 and 33 through 37 are withdrawn from consideration as being directed to a non-elected invention.

Claims 1 through 6, 12 through 19, 25 through 32, 38 and 39 were rejected.

This amendment is in response to the final Office Action of May 21, 2003.

Applicant notes the filing of three Information Disclosure Statements on June 29 1999, August 23, 1999 and January 27, 2000, respectively, and notes that copies of the PTO-1449 were not returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 be made of record herein.

Claims 1, 12 through 14, 25 through 27, 38 and 39 are rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshigai (U.S. Patent 5,606,199).

Claims 2 through 6, 15 through 19 and 28 through 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshigai as applied to claims 1, 12 through 14, 25 through 27, 38 and 39 above, and further in combination with Applicant's admitted prior art.

35 U.S.C. § 102(b) Rejections

Anticipation Rejection Based on United States Patent 5,606,199 to Yoshigai

Claims 1, 12 through 14, 25 through 27, 38 and 39 are rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent 5,606,199, issued to Yoshigai (hereinafter Yoshigai). Applicant respectfully traverses this rejection.

Applicant submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Yoshigai reference describes a lead frame with an island 7 suspended by four suspending pins 8, with a central recess 7a as a chip support section in which the semiconductor

chip 4 is mounted. Ground leads 3G of the tape carrier connect electrode pads 4a of the chip 4 and inner lead sections 6a of corresponding lead frame leads 6. Each of the ground leads 3G has two branch leads 3d which are connected to different portions of an island 7 of the lead frame.

Claim 1, as proposed to be amended herein, recites a semiconductor device assembly with a paddle of a lead frame having side rails and cross members connected to the paddle by paddle support bars with the paddle. Independent claim 14, as proposed to be amended herein, recites a planar metal paddle attached to at least one side rail by at least a plurality of paddle support bars with said metal paddle and being attached to a plurality of cross members by said support bars. Independent claim 27, as proposed to be amended herein, recites a metallic paddle secured to said second surface of said semiconductor die, said metallic paddle being attached to at least one side rail by at least a plurality of paddle support bars with said metallic paddle and being attached to a plurality of cross members by said support bars.

Applicant submits that Yoshigai fails to describe each and every element of amended independent claims 1, 14, and 27. Specifically, the reference fails to disclose the element of the presently claimed invention calling for a paddle of a lead frame having side rails and cross members connected to the paddle with paddle support bars. Figure 2 clearly shows ground leads 3G residing in a different plane from LF leads 6, branch leads 3d in another plane, supporting island 7 with central recess 7a in yet another plane.

Applicant further submits that the Yoshigai reference fails to describe the element of the claimed invention of amended independent claims 1, 14, and 27 of at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die for direct connection to a substrate, the projections including one of at least one solder ball and solder bump. The Yoshigai reference describes electrode pads 4a connected to inner lead sections 3a of the copper foil leads 3. Outer lead sections 3b of the copper foil leads are bonded, not to a substrate, but to inner lead sections 6a of the LF leads 6.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), Yoshigai does not anticipate each and every element of any of independent claims 1, 14, and 27.

Each of claims 12, 13, 25, 26, 38 and 39 is respectively allowable, among other reasons, as depending from claims 1, 14, and 27, which are allowable.

Dependent claims 12, 25, and 38 are additionally allowable because Yoshigai fails to describe an assembly including a substrate having circuit connections, with bond pads bonded to the circuit connections. Therefore, Applicant requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b).

35 U.S.C. § 103(a) Rejections

Obviousness Rejection Based on United States Patent 5,606,199 to Yoshigai in View of Applicant's Admitted Art

Claims 2 through 6, 15 through 19 and 28 through 32 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshigai as applied to claims 1, 12 through 14, 25 through 27, 38 and 39 above, and further in combination with Applicant's admitted prior art.

Applicant submits that the combination of these references does not teach or suggest the presently claimed invention.

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

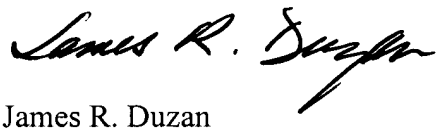
Each of claims 2 through 6, 15 through 19 and 28 through 32 is respectively allowable, among other reasons, as depending from claims 1, 14, and 27, which are each allowable.

CONCLUSION

For the reasons set forth hereinabove, Applicant submits that claims 1 through 39 are clearly allowable over the cited prior art.

Applicant requests the entry of this amendment, the allowance of claims 1 through 39, and the case passed for issue.

Respectfully submitted,



James R. Duzan
Registration No. 28,393
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: October 13, 2003
JRD/sls:djp
Document in ProLaw

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device assembly of a plurality of semiconductor device assemblies, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die ~~directly connected~~ for direct connection to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and

a generally centrally positioned paddle of a lead frame of a plurality of lead frames having side rails and cross members connected to said paddle, said second surface of said semiconductor die being secured to said paddle; and said ~~generally centrally positioned~~ paddle being attached to the side rail by at least a plurality of paddle support bars and being attached to said cross members by said support bars.

2. (Original) The semiconductor device assembly of claim 1, wherein said at least one projection includes a plurality of projections comprising a ball grid array (BGA) of solder balls.

3. (Original) The semiconductor device assembly of claim 1, wherein said at least one projection comprises at least one ball deposited by a wire bonding machine.

4. (Original) The semiconductor device assembly of claim 1, wherein said at least one projection comprises at least one stud bump deposited by a wire bonding machine.

5. (Previously Presented) The semiconductor device assembly of claim 1, further comprising:

an electrically non-conductive adhesive layer securing said second surface to said generally centrally positioned paddle.

6. (Original) The semiconductor device assembly of claim 5, wherein said adhesive layer comprises one of epoxy and polyimide.

7. (Withdrawn) The semiconductor device assembly of claim 1, further comprising:

an electrically conductive adhesive layer securing said second surface of said semiconductor die to said generally centrally positioned paddle.

8. (Withdrawn) The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a eutectic material.

9. (Withdrawn) The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a gold-silicon eutectic material.

10. (Withdrawn) The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductive material.

11. (Withdrawn) The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises conductive polyimide.

12. (Original) The semiconductor device assembly of claim 1, further comprising:

said substrate having circuit connections, said plurality of bond pads bonded to said circuit connections.

13. (Original) The semiconductor device of claim 12, further comprising:
sealant packaging material enclosing a portion of said semiconductor die and covering a portion of said substrate.

14. (Currently Amended) A semiconductor device assembly of a plurality of semiconductor device assemblies, comprising:
a semiconductor die having an active surface having at least one bond pad thereon and an opposing second surface;
at least one projection secured to said at least one bond pad on said active surface of said semiconductor die ~~directly connected~~ connected to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and
a metal paddle from a lead frame, said second surface of said semiconductor die being attached to said paddle; and said metal paddle is attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

15. (Original) The semiconductor device assembly of claim 14, wherein said at least one projection comprises a ball grid array (BGA) of solder balls.

16. (Original) The semiconductor device assembly of claim 14, wherein said at least one projection comprises at least one ball deposited by a wire bonding machine.

17. (Original) The semiconductor device assembly of claim 14, wherein said at least one projection comprises at least one stud bump deposited by a wire bonding machine.

18. (Original) The semiconductor device assembly of claim 14, further comprising:
an electrically non-conductive adhesive layer attaching said second surface to said paddle.

19. (Original) The semiconductor device assembly of claim 18, wherein said adhesive layer comprises one of epoxy and polyimide.

20. (Withdrawn) The semiconductor device assembly of claim 14, further comprising: an electrically conductive adhesive layer attaching said second surface to said metal paddle.

21. (Withdrawn) The semiconductor device assembly of claim 20, wherein said electrically conductive adhesive layer comprises a eutectic material.

22. (Withdrawn) The semiconductor device of claim 20, wherein said electrically conductive adhesive layer comprises a gold-silicon eutectic material.

23. (Withdrawn) The semiconductor device assembly of claim 21, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductor.

24. (Withdrawn) The semiconductor device assembly of claim 21, wherein said electrically conductive layer comprises conductive polyimide.

25. (Original) The semiconductor device assembly of claim 14, further comprising: a substrate having a plurality of circuit connections, said at least one bond pad connected to at least one circuit connection of said plurality of circuit connections.

26. (Original) The semiconductor device assembly of claim 25, further comprising: sealant packaging covering a portion of said semiconductor die and a portion of said substrate.

27. (Currently Amended) A semiconductor device assembly <u>of a plurality of semiconductor device assemblies</u>, comprising:
a semiconductor die having an active surface having a plurality of bond pads thereon and an

opposing second surface;

a plurality of projections connected to said plurality of bond pads ~~directly connected~~ for direct connection to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps; and

a metallic paddle secured to said second surface of said semiconductor die, said metallic paddle being attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

28. (Original) The semiconductor device assembly of claim 27, wherein said plurality of projections comprises a ball grid array (BGA) of solder balls.

29. (Original) The semiconductor device assembly of claim 27, wherein said plurality of projections comprises balls deposited by a wire bonding machine.

30. (Original) The semiconductor device assembly of claim 27, wherein said plurality of projections comprises a plurality of stud bumps deposited by a wire bonding machine.

31. (Previously Presented) The semiconductor device assembly of claim 27, further comprising:

an electrically non-conductive adhesive layer connecting said second surface to said metallic paddle.

32. (Original) The semiconductor device assembly of claim 31, wherein said adhesive layer comprises one of epoxy and polyimide.

33. (Withdrawn) The semiconductor device assembly of claim 27, further comprising:

an electrically conductive adhesive layer connecting said second surface to said metallic paddle.

34. (Withdrawn) The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a eutectic material.

35. (Withdrawn) The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a gold-silicon eutectic material.

36. (Withdrawn) The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductive material.

37. (Withdrawn) The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises conductive polyimide.

38. (Original) The semiconductor device of claim 27, further comprising:
a substrate having a plurality of circuit connections, said plurality of bond pads connected to said plurality of circuit connections.

39. (Original) The semiconductor device assembly of claim 38, further comprising:
sealant packaging covering a portion of said semiconductor die and a portion of said substrate.